AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A method of performing a context switch operation, the method comprising:

setting an index register on an address portion of a state machine in a peripheral system to a first index value by a host computer, the first index value indicating a first register to be accessed;

in response to setting the index register to the first index value, accessing context data in the first register of the peripheral system based upon the first index value;

setting the index register to a second index value by the host computer, the second index value indicating a second register to be accessed; and

in response to setting the index register to the second index value, accessing context data in the second register of the peripheral system ~~when the index register is set to~~ based upon the second index value, wherein the first and second registers are collocated with the peripheral system.~~,~~

~~wherein setting the index register to the first index value, accessing the context data in the first register, setting the index register to the second index value and accessing context data in the second register are performed in accordance with a state transition diagram.~~

2. (Previously Presented) The method recited in claim 1, wherein the context data includes:

a device address for one of a plurality of network devices;

a class value;

a clock offset value; and

an active member address.

3. (Previously Presented) The method recited in claim 1, wherein-accessing the context data in the second register comprises:

receiving, by the peripheral system, an address value that identifies an address within the second register;

receiving, by the peripheral system, a control input that identifies at least one of a plurality of functions, the plurality of functions including a read function and a write function;

receiving, by the peripheral system if the control input identifies the write function, a data value; and

if the control input identifies the write function, writing the data value to the second register at the address identified by the address value.

4. (Previously Presented) The method recited in claim 1, wherein accessing the context data in the second register comprises:

receiving, by the peripheral system, an address value that identifies an address within the second register;

receiving, by the peripheral system, a read control input; and

providing the contexts of the second register at the address identified by the address value to the host computer.

5. (Previously Presented) The method recited in claim 1, wherein accessing the context data in the second register comprises:

receiving, by the peripheral system, an address value that identifies an address within the second register;

receiving, by the peripheral system, a data value;

receiving, by the peripheral system, a write control input; and

writing the data value to the second register at the address identified by the address value.

6. (Previously Presented) The method recited in claim 1, wherein accessing context data in the second register comprises:

receiving, by the peripheral system, an address value that identifies an address within the second register;

receiving, by the peripheral system, a control input that identifies one of a plurality of functions, the plurality of functions including a read function and a write function; and

if the control input identifies the read function, providing the contents of the second register at the address identified by the address value to the host computer.

7. (Original) The method recited in claim 1, wherein the first and second registers are not architected registers.

8. (Currently Amended) A system, comprising:

a host computer, the host computer including a microprocessor;

at least one peripheral system coupled to the host ~~processor~~ computer, the peripheral system including a state machine including an index register, the peripheral system further including a first register, the first register being associated with a first index value, the peripheral system further including a second register, the second register being associated with a second index value, wherein the first and second registers are collocated with the peripheral system;

an interface coupled to the host computer and to the peripheral system, the interface being configured to provide the first and second index values from the host computer to the peripheral system; and

a register access circuit in the peripheral system, the register access circuit being configured to access context data in the first register ~~when~~ in response to the first index value ~~is~~ being provided by the host computer, wherein the index register is configured to store either of the first and second index values, the register access circuit being further configured to access context data in the second register ~~when~~ in response to the second index value ~~is~~ being provided by the host computer.~~,~~

~~and wherein the register access circuit accesses context data in the first and second registers in accordance with a state transition diagram.~~

9. (Previously Presented) The system recited in claim 8, wherein the first and second registers are not architected registers.

10. (Original) The system recited in claim 8, wherein the peripheral system includes a state machine module, the state machine module including:

an address portion;

a control portion; and

a data portion, the first register and the second register being included in the data portion.

11. (Original) The system recited in claim 8, wherein the peripheral system includes a microprocessor.

12. (Previously Presented) The system recited in claim 10, wherein the address portion comprises the register access circuit.

13. (Previously Presented) The system recited in claim 8, wherein the peripheral system includes a plurality of context registers, wherein each of the plurality of context registers is associated with one of a plurality of index values other than the first and second index values.

14-20. (Canceled)